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**REMARKS**

Applicant has carefully reviewed and considered the Office Action mailed on December 10, 2002, and the references cited therewith.

Claims 1, 6, 7, 13, 14, 21-23, 29, 30, 41, 74, 77, 79, and 82 are amended; as a result, claims 1-49, and 74-84 are now pending in this application.

*Affirmation of Election*

Applicant hereby affirms election of claims 1-49 and 74-84, and cancellation of claims 50-73 as expressed in the response to the restriction requirement that Applicant sent on October 24, 2002.

*Claims objections*

Claim 77 is objected because of informalities. Claim 77 is amended to correct the informalities as suggested in the Office Action.

*§112 Rejection of the Claims*

Claims 6-29 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

In claims 6-29, claims 6, 13, and 22 are independent claims and other claims are dependent claims. Independent claims 1, 13, and 22 are amended. As amended, claims 6, 13, and 22 particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Therefore, Applicant respectfully requests that the rejection of claims 6-29 be reconsidered and withdrawn.

*§102 Rejection of the Claims*

Claims 1-19, 21-27, 29-38, 40-47, 74, and 76-84 were rejected under 35 USC § 102(b) as being anticipated by Nishimichi (U.S. 5,287,025).

Nishimichi discloses a timing control circuit for applying a delay to an external clock signal to generate an internal clock signal. When the external and internal clock signals *are not*

synchronized, a shift register changes the delay to synchronize external and internal clock signals. When the external and internal clock signals *are* synchronized, the shift register does not change the delay.

The features of the timing control circuit of Nishimichi and the features of the present invention are different and perform different functions.

Claim 41 of the invention recites a delay locked loop comprising delay stages for applying an amount of delay to an external clock signal to generate a first delayed signal and a second delayed signal. Claim 41 also recites a "selector" connected to the delay stages for selecting the first delayed signal to be an internal clock signal, wherein the external and internal clock signals "are synchronized".

Claim 41 is amended to clarify that the selector replaces the first delayed signal with the second delayed signal "while" the external and internal clock signals "are synchronized".

In contrast, Nishimichi discloses a shift register to control a selecting circuit for selecting from among different signals *while* the external and internal clock signals are *not* synchronized. Fig. 1, Fig. 5, Fig. 8, and Fig. 9 of Nishimichi show a shift register 50 for controlling a selecting circuit 40 to select from among the signals on lines 34a-34h and 35a-35h to adjust an amount of delay. Fig. 2, Fig. 7, and Fig. 10 show that while the external and internal clock signals are not synchronized, shift clock 54 causes shift register 50 to shift to adjust the amount of delay until the external and internal clock signals are synchronized. When the external and internal clock signals are synchronized, shift clock 54 remains at the same level and selecting circuit 50 *does not* replace the internal clock signal with a different signal. Thus, Nishimichi does not disclose a "selector" for replacing a first delayed signal with a second delayed signal "while" the external and internal clock signals "are synchronized".

Based on the differences presented above, Nishimichi does not disclose all of the features recited in claim 41. Therefore, claim 41 is not anticipated by Nishimichi. Applicant requests that the rejection of claim 41 be reconsidered and withdrawn and that claim 41 and its dependent claims be allowed.

Independent claims 1, 6, 13, 22, 30, 74, 79, and 82 are amended. These claims, as amended, recite features similar to the features of claim 41. Thus, these claims are also not

anticipated by Nishimichi for reasons similar to the reasons presented above regarding claim 41.

Therefore, Applicant requests that the rejection of claims 1, 6, 13, 22, 30, 74, 79, and 82 be reconsidered and withdrawn and that these claims and their dependent claims be allowed.

*§103 Rejection of the Claims*

Claims 20, 28, 39, 48, 49, and 75 were rejected under 35 USC § 103(a) as being unpatentable over Nishimichi.

Claims 20, 28, 39, 48, 49, and 75 depend on independent claims 13, 22, 30, 41, and 74. Based on the differences presented above regarding the independent claims, claims 20, 28, 39, 48, 49, and 75 are also patentable over Nishimichi because they depend on the patentable independent claims. Thus, Applicant requests that the rejection of claims 20, 28, 39, 48, 49, and 75 be reconsidered and withdrawn and that these claims be allowed.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative (612-373-6969) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

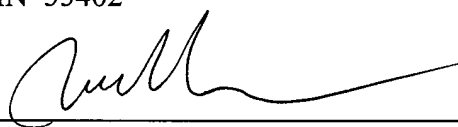
Respectfully submitted,

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Date 3-10-03

By 

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 10th day of March, 2003.

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